

GIET POLYTECHNIC, JAGATPUR, CUTTACK

LESSON PLAN

Discipline: ELECTRICAL	Semester: 5 th	Name Of The Teaching Faculty: SUGANDHA PUSPITA MADHUJHARA
Subject: DE&MP (TH- 03)	No. Of Days Per Week Class Allotted: 05 P	Semester From Date: 01.07.2024 To Date: 08.11.2024 No. of weeks: 15
Week	Class Day	Theory Topic
1" week	1 st	> 1. BASICS OF DIGITAL ELECTRONICS
	2 nd	 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	3 rd	 Binary addition, subtraction, Multiplication and Division.
	4 th	Subtraction of binary numbers in 2's complement method.
	5 th	 Use of weighted and Un-weighted codes & write Binary equivalent number
2 nd week	1 st	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	2 nd	 Realize AND, OR, NOT operations using NAND gates
	3 rd	> Realize AND, OR, NOT operations using NAND gates
	4 th	 Different postulates and De-Morgan's theorems in Boolean algebra.
	5 th	 Use Of Boolean Algebra For Simplification Of Logic Expression
3º week	1 st	 Use Of Boolean Algebra For Simplification Of Logic Expression
	2 nd	 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	3rd	 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	4 th	- 2. COMBINATIONAL LOGIC CIRCUITS
	5 th	Half adder circuit and verify its functionality using truth table
4 th week	1st	Realize a Half-adder using NAND gates only and NOR gates only.
	2 nd	Full adder circuit and explain its operation with truth table.
	3 rd	 Realize full-adder using two Half-adders and an OR – gate and write truth table
	4 th	 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	5 th	 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
5° week	1 st	- Working of Binary-Decimal Encoder & 3 X 8 Decoder

1	2 nd	Pin diagram and description.
	3 rd	INTERNAL TEST
	4 th	> Stack, Stack pointer & stack top
	5 th	> Interrupts
12 th week	181	Instruction set of 8085 example
	2 nd	Instruction set of 8085 example
	3 rd	 Addressing mode
	4 th	 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5 th	 Timing Diagram for memory read, memory write, I/O read, I/O write
	185	 Timing Diagram for 8085 instruction
	2 nd	Counter and time delay
13th week	3rd	Simple assembly language programming of 8085
	4 th	INTERFACING AND SUPPORT CHIPS
	5 th	 Basic Interfacing Concepts, Memory mapping & I/O mapping
	1 st	interface Intel 8255
(14 th week	2 nd	 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	3 rd	 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	4 th	 Application using 8255: Seven segment LED display, Square wave generator, Trafficlight Controller
	5 th	REVISION
	118	 Application using 8255: Seven segment LED display, Square wave generator, Trafficlight Controller
-	2 ^{od}	Constant – K Band elimination filter
15" week	3 rd	> SOLVE NUMERICAL PROBLEMS
	41%	> REVISION
	5 th	> REVISION

29/06/24 Signature of faculty

Signature of Sr. Jacober
Head of Dept.
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Signature of Principal